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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Dominik J. Schmidt	§	Group Art Unit:	2181
Serial No.:	10/690,263	§	Examiner:	Richard Franklin
Filed:	October 21, 2003	§		
For:	Integrated Circuit Capable Of Working With Multiple Bus Interface Standards	§	Atty. Dkt. No.:	IVT.0032US

Mail Stop **Appeal Brief - Patents**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDED APPEAL BRIEF TRANSMITTAL

Sir:

Transmitted herewith is the Amended Appeal Brief for this application. The Appeal Brief was filed on April 3, 2007.

Pursuant to M.P.E.P. § 1205.03, there is no fee due for this Appeal, because the Examiner requested that the Appellant file a new Appeal Brief in compliance with 37 CFR 41.37(c) after filing of the Appeal Brief on April 3, 2007. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504.

Respectfully submitted,

Date: 7/30/07

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I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as **first class mail** with sufficient postage on the date indicated above and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Stephanie Petreas

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Stephanie Petreas

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I. REAL PARTY IN INTEREST

The real party in interest is the assignee Gallitzin Allegheny LLC, the assignee of the present application by virtue of the assignment recorded at Reel/Frame 015271/0226.

II. RELATED APPEALS AND INTERFERENCES

A previous Appeal was filed for this application on September 13, 2006; however, prosecution was re-opened on November 17, 2006. Otherwise, there are no related appeals and interferences.

III. STATUS OF CLAIMS

Claims 1-10 stand rejected and claims 11-20 are canceled. The rejections of pending claims 1-10 are being appealed.

IV. STATUS OF AMENDMENTS

All amendments have been entered, including the amendment filed in the Reply to Final Office Action of November 17, 2006, subsequent to the final rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Claim 1 is an independent claim. [1] Support for claim 1 is set forth, for example, in the Specification at page 4, lines 3-8, which sets forth the recited first interface circuit, second interface circuit, and common set of pins. Additional support for these elements of claim 1 can be found in regard to FIG. 2 and the corresponding portions of the Specification. Specifically, FIG. 2 shows an interface circuit that includes first and second interface circuits, e.g., a first signal translator 80 and a second signal translator 90, which are part of an add-on card 60 that includes a group of pins, i.e., a common set of pins that are coupled to both of the signal translators to communicate with a host input/output bus 70. Specification, p. 8, ln. 4 – p. 9, ln. 5; FIG. 2.

Claim 8 is an independent claim. Support for claim 8 is set forth, for example, in the Specification at page 4, lines 3-8 and page 8, line 3 – page 9, line 5, which sets forth the recited first interface circuit, second interface circuit, common set of pins, and internal bus. Additional support for these elements of claim 8 can be found in regard to FIG. 2 and the corresponding portions of the Specification. Specifically, FIG. 2 shows an interface circuit that includes first and second interface circuits, e.g., a first signal translator 80 and a second signal translator 90, which are part of an add-on card 60 that includes a group of pins, i.e., a common set of pins that are coupled to both of the signal translators to communicate with a host input/output bus 70. FIG. 2 also shows an internal bus 95 coupled to the first and second signal translators. Specification, p. 8, ln. 4 – p. 9, ln. 5; FIG. 2.

Claim 10 is an independent claim. Support for claim 10 is set forth, for example, in the Specification at page 4, lines 3-8, page 8, line 3 - page 9, line 5, and page 9, line 21 – page 10, line 6, which sets forth the recited first interface circuit, second interface circuit, common set of pins, and power supplies. Additional support for these elements of claim 10 can be found in regard to FIG. 2 and the corresponding portions of the Specification. Specifically, FIG. 2 shows an interface circuit that includes first and second interface circuits, e.g., a first signal translator 80 and a second signal translator 90, which are part of an add-on card 60 that includes a group of

[1] It is respectfully noted that the Examiner required the filing of this Amended Appeal Brief, as the Examiner stated that "Each limitation of each independent claim must be concisely mapped to the specification by page and line number and to the drawings by reference numeral." Notice of Non-Compliant Appeal Brief, mailed July 10, 2007. However, 37 C.F.R. §41.37(c)(1)(v) nowhere requires such mapping of "each limitation." 37 C.F.R. §41.37(c)(1)(v). Nevertheless, in the interest of moving this Appeal Brief forward, Applicants provide the requested information herewith.

pins, i.e., a common set of pins that are coupled to both of the signal translators to communicate with a host input/output bus 70. FIG. 2 also shows an internal bus 95 coupled to the first and second signal translators. Furthermore, FIG. 4 shows the recited first and second power supplies, namely a first power supply 302 and a second power supply 304. Specification, p. 8, ln. 4 – p. 9, ln. 5; p. 9, ln. 21 – p. 10, ln. 6; FIGS. 2 and 4.

Embodiments of the present invention thus include an interface circuit that conforms to multiple bus standards. The interface circuit includes a first interface circuit conforming to a first bus standard, a second interface circuit conforming to a second bus standard, and a common set of pins coupled to the first and second interface circuits that are user selectable to communicate with a host computer bus in accordance with either of the first or second bus standards.

In this way, the circuit shares the pins of an IC to be field programmed to use a common set of pins to both transmit and receive data conforming to either a PCI bus standard or a PCMCIA bus standard. Based on a programmable chip setting, each bus interface pin can be used to communicate over a plurality of bus interface definitions such as PCI and PCMCIA bus definitions. One interface IC can be used to handle multiple bus standards. For example, one IC can handle either the PCI interface or the PCMCIA interface to avoid the need to keep two versions of the same IC in inventory. Specification, p. 4, lns. 3-17.

Referring to FIG. 1 there is shown a peripheral device 10 connected to a computer 12. The device 10 can perform any peripheral functions. For example, it can be a wireless communication IC, a solid state storage IC, among others. In the preferred embodiment, it interfaces with a computer 12 in accordance with either the PCI or the PCMCIA standard, depending on a user selectable indication such as an input pin of the device 10 or a bit in a register that can be programmed. In either case, the device 10 receives address signals from the computer 12 on an address bus 14 and control signals on a control bus 18, and in response thereto provides data signals on a data bus 16 to the computer 12. Thus, in the preferred embodiment, the device 10 provides two modes of operation. In one mode of operation, the computer 12 communicates with the device 10 over a PCI bus. In another mode of operation, the device 10 communicates with the computer 12 over a PCMCIA bus. Specification, p. 7, ln. 14 – p. 8, ln. 2.

FIG. 2 shown an exemplary connection between a host computer 50 that accepts an add-on card 60 plugged into a host input/output bus 70. Within the add-on card 60, signals from the bus 70 communicate with a plurality of I/O buffers 62. In one embodiment, the I/O buffers 62 are multi-voltage I/O buffers than can handle different voltage levels such as 5 volts, 3 volts, or 1 volt signals, for example. The buffers allow the I/O pins or bi-directional pins to handle an input voltage that is greater than the DC supply voltage for the electronics of the I/O pins. For example, the DC supply voltage can be 3.3V but the device may have to receive an input signal that reaches a value of 5V from another device that has a DC supply voltage of 5V. The circuit accepts various logic level inputs form a bus that conforms to one of a plurality of bus standards (such as PCI or PCMCIA). This is done while reducing normal power consumption associated with receiving the various logic levels. The system can output at a group of pins one set of logic levels (such as PCI levels) and, when configured, can output at the same group of pins a different set of logic levels (such as PCMCIA levels). Specification p. 8, lns. 3-16.

The I/O buffers 62 in turn communicate with a signal translator 75 that includes a first signal translator 80, a second signal translator 90, and additional signal translators if needed. The signal translators 80 and 90 are also connected to an internal bus 95 on the card 60. One or more peripheral circuits 98 can be connected to the bus 95 to provide the functionality associated with the add-on card. Specification, p. 8, lns. 17-21.

FIG. 3 shows a first embodiment of an exemplary member of a multi-voltage I/O buffer 62. A multi-voltage I/O buffer 200 is provided with its input supply rails tied to one input of a switch SW. The second input of the switch SW is tied to one end of a pull-up resistor 202. The other end of the pull-up resistor 202 is tied to a high voltage supply rail. During operation, the user can select the switch to be in its open or closed state. In its open state, the rail voltage of the buffer 200 rises to a first supply rail voltage, while in its closed state, the rail voltage of the buffer 200 rises to a second supply rail voltage, as determined by the pull-up resistor 202.

FIG. 4 shows a second embodiment of an exemplary multi-voltage I/O buffer 62. In this embodiment, a buffer 300 (which can be unidirectional or bidirectional) has a voltage input connected to a switch SW1. One input of the switch SW1 is connected to a first power supply regulator 302, while the second input of the switch SW1 is connected to a second power supply regulator 304. Switch SW1 toggles between the first and second power supply regulators 302

and 304 to connect the voltage input to different input voltages for the buffer 300. Specification, p. 9, ln. 13 – p. 10, ln. 4.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Each of the following grounds of rejection are presented for review:

(1) claims 1-2 and 5-6 stand rejected under 35 U.S.C. § 102(b) over Moss

A. claims 1 and 2 stand rejected under 35 U.S.C. § 102(b) over Moss

B. claim 5 stands rejected under 35 U.S.C. § 102(b) over Moss

C. claim 6 stands rejected under 35 U.S.C. § 102(b) over Moss

(2) claims 3 and 4 stand rejected under 35 U.S.C. § 103(a) over Moss in view of Tyson

(3) claim 7 stands rejected under 35 U.S.C. § 103(a) over Moss

(4) claim 8 stands rejected under 35 U.S.C. § 103(a) over Moss

(5) claim 9 stands rejected under 35 U.S.C. § 103(a) over Moss and Cahill

(6) claim 10 stands rejected under 35 U.S.C. § 103(a) over Moss and Cahill

VII. ARGUMENT

(1) Claims 1-2 and 5-6 Are Patentable Under 35 U.S.C. § 102(b) over Moss

A. Claims 1 and 2 Are Patentable Under 35 U.S.C. § 102(b) over Moss

Claims 1 and 2 stand rejected under 35 U.S.C. §102(b) over U.S. Patent No. 5,793,989 (Moss). This rejection is improper and should be reversed. Claim 1 is an independent claim reciting an interface circuit that conforms to multiple bus standards and including a first interface circuit conforming to a first bus standard, a second interface circuit conforming to a second bus standard, and a common set of pins coupled to the first and second interface circuits and a host computer bus, where the common set of pins are user selectable to communicate with the host computer bus in accordance with either of the first or second bus standards.

The rejection as to claim 1 is improper, at least because Moss nowhere teaches: (1) a common set of pins coupled to first and second interface circuits and a host computer bus; (2) such common set of pins communicating with the host computer bus in accordance with either a first or second bus standard; or (3) the common set of pins being user selectable.

As to point (1), the Examiner contends that the common set of pins is taught by Moss as element 105 (*see* Final Office Action mailed November 17, 2006 (hereafter Final Office Action), p. 5), which Moss teaches is a female mechanical connector. Moss, col. 2, lns. 32-33. However, this connector is not coupled to both multiple interface circuits *and* a host computer bus. In fact, this female connector is not coupled to either of the multiple interface circuits or host computer bus in Moss. In this regard, the Examiner contends that the interface circuits are met by PCMCIA logic 112 and alternate interface logic 113 of Moss, while the recited host computer bus is met by an I/O bus 127. Final Office Action, p. 5. However, female connector 105 is not coupled to any of these elements of Moss, contrary to the Examiner's contention. Instead, Moss teaches that the connector 105 is connected to a card logic unit 111 and a corresponding mechanical connector 107 of an applications device 103. *E.g.*, Moss, Fig. 1. As such, the peripheral device 101 of which connector 105 is a part is not coupled to a host computer bus. Instead, it is simply coupled to the applications device 103. Accordingly, Moss fails to teach a common set of pins coupled to both of multiple interface circuits and a host computer bus.

Furthermore, as to point (2) Moss nowhere teaches that such (non-existent) common pins communicate with the host computer bus in accordance with either of the first or second bus

standards. In fact, Moss teaches absolutely the opposite. That is, in Moss only RS-232 signals are communicated with I/O bus 127 (contended by the Examiner to be the computer bus). Moss, col. 1, lns. 29-31. Because claim 1 recites that communication with a host computer bus is to be in accordance with either of two bus standards, the permanent RS-232 connection to I/O bus 127 taught in Moss cannot meet the claimed subject matter.

As to point (3), the Examiner further contends that the common set of pins of Moss is user selectable "because the user ultimately in the end selects the pin format." Final Office Action, p. 4. This contention is nothing but unsupported argument by the Examiner, as nothing in Moss anywhere teaches or suggests such "ultimate user selection." That is, in Moss there is no mention of a user, nor that the user makes a selection of a bus standard with which common pins communicate with a host computer bus. Furthermore, the Examiner appears to concede that it is not a user that makes the selection: instead, the Examiner contends that it is socket logic unit 109 of the applications device 103 that "represents the 'user selectable' function...." Final Office Action, p. 4. However, all that Moss teaches with regard to socket logic 109 is that a unique code can be set or presented. However, nowhere does Moss teach that such code be user set. Furthermore, no matter how socket logic unit 109 is set, communication with the host computer bus is still only with regard to a single bus standard. That is, as described above, there is no communication with a host computer bus in Moss in accordance with multiple bus standards. Accordingly, the rejection of claim 1 and claim 2 depending therefrom is improper and should be reversed.

B. Claim 5 Is Patentable Under 35 U.S.C. § 102(b) Over Moss

Claim 5 depends from claim 1 and further recites a multi-voltage input/output buffer coupled to each pin. Claim 5 stand rejected under 35 U.S.C. § 102(b) over Moss. The rejection of dependent claim 5 is improper at least for the same reasons discussed regarding claim 1 (*see* VII.1.A.).

The rejection of claim 5 is further improper, as Moss nowhere teaches a multi-voltage I/O buffer coupled to each pin. Instead, the Examiner merely refers in Moss to tri-state buffers that act as multiplexing switches within card logic unit 111. Such multiplexing switches are clearly not multi-voltage I/O buffers.

C. Claim 6 Is Patentable Under 35 U.S.C. § 102(b) Over Moss

Claim 6 depends from claim 1 and further recites an internal bus that is coupled to both first and second interface circuits. The rejection of claim 6 is improper at least for the same reasons discussed above regarding claim 1 (*see* VII.1.A). The rejection of dependent claim 6 is further improper as Moss nowhere teaches an internal bus coupled to *both* first and second interface circuits. In this regard, the Examiner refers to items 114, 115, 116 and 119 of Moss as internal buses. However, as clearly taught and shown in Moss, each of these buses are independent buses and no one of these buses couples to both interface circuits. Moss, FIG. 1. Clearly, as shown in FIG. 1 of Moss, buses 114 and 115 only communicate with alternate interface logic 113 and never with PCMCIA logic 112. Similarly, buses 116 and buses 119 communicate only with PCMCIA logic 112 and never with alternate interface logic 113. Accordingly, Moss fails to teach a single internal bus that is coupled to multiple interface circuits, as recited by claim 6. For this further reason, the rejection of claim 6 is improper and should be reversed.

(2) Claims 3 and 4 Are Patentable Under 35 U.S.C. § 103(a) Over Moss in view of Tyson

Claim 3 depends from claim 1 and further recites that the first bus standard comprises a PCI standard. Claim 3 stands rejected under 35 U.S.C. § 103(a) over Moss in view of Tyson "How PCI Works." This rejection is improper at least for the same reasons described above regarding claim 1 (*see* VII.I.A.). Furthermore, while Tyson teaches that computers can use a PCI bus to connect peripherals, there is no suggestion or motivation to combine such a bus with the peripheral device of Moss. In this regard, "the mere fact that references can be combined or modified does not render the resulting combination obvious unless the prior art also suggests the desirability of the combination." *In re Mills,* 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990). As such, the rejection of claim 3 (and claim 4 depending therefrom) is clearly erroneous as neither reference provides any rationale suggesting the desirability of the combination. MPEP §2143.01.

(3) Claim 7 Is Patentable Under 35 U.S.C. § 103(a) Over Moss

Dependent claim 7 depends from claim 6, which in turn depends from claim 1. Claim 7 further recites that the first interface circuit is configured to format signals on the internal bus to

signals compliant with the first bus standard. This rejection of claim 7 under §103(a) over the single reference Moss is improper at least for the same reasons discussed above regarding claims 1 and 6 (*see* VII.1.A. and C.).

The rejection is further erroneous, as there is no teaching or suggestion in Moss to somehow modify itself to provide an interface circuit that formats signals on an internal bus that is coupled to both interface circuits. Instead in Moss, dedicated buses exist, namely dedicated buses 114 and 116 and dedicated buses 115 and 119, each of which provides signals of only a single bus standard to the corresponding interface circuit. Accordingly, the rejection of claim 7 is improper and should be reversed.

(4) Claim 8 Is Patentable Under 35 U.S.C. § 103(a) Over Moss

Independent claim 8 stand rejected under 35 U.S.C. § 103(a) over Moss. This rejection is improper and should be reversed. Claim 8 recites an interface circuit that conforms to multiple bus standards and including a first interface circuit conforming to a first bus standard, a second interface circuit conforming to a second bus standard, and a common set of pins coupled to the first and second interface circuits and a host computer bus, where the common set of pins are user selectable to communicate with the host computer bus in accordance with either of the first or second bus standards. Furthermore, claim 8 includes an internal bus coupled to the interface circuits, where the first interface circuit is configured to format signals on the internal bus to signals compliant with the first bus standard and the second interface circuit is configured to format signals on the internal bus compliant with the second bus standard.

As described above regarding claim 6 (*see* VII.1.C). Moss fails to teach or suggest an internal bus coupled to both first and second interface circuits. Furthermore, Moss fails to teach the common set of pins coupled to first and second interface circuits and a host computer bus, communication with the host computer bus in accordance with either first or second bus standards, or user selectable common pins.

The rejection is further erroneous, as there is no teaching or suggestion in Moss to somehow modify itself to provide an interface circuit that formats signals on an internal bus that is coupled to both interface circuits. Instead in Moss, dedicated buses exist, namely dedicated buses 114 and 116 and dedicated buses 115 and 119, each of which provides signals of only a

single bus standard to the corresponding interface circuit. Accordingly, the rejection of claim 8 should be reversed.

(5) Claim 9 Is Patentable Under 35 U.S.C. § 103(a) Over Moss and Cahill

Claim 9 depends from claim 1 and further recites a first power supply to supply voltage swings in accordance with the first bus standard. Claim 9 stands rejected under 35 U.S.C. § 103(a) over Moss in view of U.S. Patent No. 6,871,244 (Cahill). The rejection of claim 9 is improper for at least the same reasons discussed above regarding claim 1 (*see* VII.1.A.). Furthermore, there is no motivation or suggestion in either of the references to combine the subject matter of Cahill with that of Moss. Accordingly, the rejection of claim 9 is improper and should be reversed.

(6) Claim 10 Is Patentable Under 35 U.S.C. § 103(a) Over Moss and Cahill

Claim 10 is an independent claim and recites an interface circuit that conforms to multiple bus standards and including a first interface circuit conforming to a first bus standard, a second interface circuit conforming to a second bus standard, and a common set of pins coupled to the first and second interface circuits and a host computer bus, where the common set of pins are user selectable to communicate with the host computer bus in accordance with either of the first or second bus standards. Furthermore, claim 10 recites first and second power supplies, each to supply voltage swings in accordance with one of the first and second bus standards.

Claim 10 stands rejected under 35 U.S.C. § 103(a) over Moss in view of Cahill. The rejection of claim 10 is improper at least for the same reasons discussed above regarding claim 1 (*see* VII.1.A.). Furthermore, there is no motivation or suggestion in either of the references to combine the subject matter of Cahill with that of Moss. Still further, neither Moss nor Cahill anywhere teach or suggest the presence of multiple power supplies each to supply voltage swings in accordance with one of multiple bus standards. Instead, Cahill merely teaches a single power supply that provides an output voltage that may be converted to different voltages. However, Cahill nowhere teaches or suggests the presence of multiple power supplies. Of course, Moss teaches nothing in this regard. Thus, the rejection of claim 10 is clearly erroneous and the rejection should be reversed.

Applicant respectfully requests that each of the final rejections be reversed and that the claims subject to this Appeal be allowed to issue.

Respectfully submitted,

Date: 7/30/07

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VIII. CLAIMS APPENDIX

The claims on appeal are:

Claim 1: An interface circuit conforming to multiple bus standards, comprising:

a first interface circuit conforming to a first bus standard;

a second interface circuit conforming to a second bus standard; and

a common set of pins coupled to the first interface circuit and the second interface circuit and a host computer bus, the common set of pins being user selectable to communicate with the host computer bus in accordance with either the first bus standard or the second bus standard.

Claim 2: The interface circuit of claim 1, wherein the common set of pins is configured to transmit and receive data conforming to either a PCI bus standard or a PCMCIA bus standard.

Claim 3: The interface circuit of claim 1, wherein the first bus standard comprises a PCI standard.

Claim 4: The interface circuit of claim 3, wherein the second bus standard comprises a PCMCIA standard.

Claim 5: The interface circuit of claim 1, further comprising a multi-voltage input output buffer coupled to each pin.

Claim 6: The interface circuit of claim 1, further comprising an internal bus coupled to the first and second interface circuit.

Claim 7: The interface circuit of claim 6, wherein the first interface circuit is configured to format signals on the internal bus to signals compliant with the first bus standard.

Claim 8: An interface circuit comprising:

a first interface circuit conforming to a first bus standard;

a second interface circuit conforming to a second bus standard;

a common set of pins coupled to the first interface circuit and the second interface circuit and a host computer bus, the common set of pins being user selectable to communicate with the host computer bus in accordance with either the first bus standard or the second bus standard; and

an internal bus coupled to the first and second interface circuit, wherein the first interface circuit is configured to format signals on the internal bus to signals compliant with the first bus standard and the second interface circuit is configured to format signals on the internal bus to signals compliant with the second bus standard.

Claim 9: The interface circuit of claim 1, further comprising a first power supply to supply voltage swings in accordance with the first bus standard.

Claim 10: An interface circuit comprising:

a first interface circuit conforming to a first bus standard;

a second interface circuit conforming to a second bus standard;

a common set of pins coupled to the first interface circuit and the second interface circuit and a host computer bus, the common set of pins being user selectable to communicate with the host computer bus in accordance with either the first bus standard or the second bus standard;

a first power supply to supply voltage swings in accordance with the first bus standard; and

a second power supply to supply voltage swings in accordance with the second bus standard.

IX. EVIDENCE APPENDIX

There was no evidence submitted during prosecution.

X. RELATED PROCEEDINGS

There are no related proceedings in this matter.